Amendments to the Specification

Please replace the paragraph that begins on page 10, line 6, with the following paragraph:

Figure 2 illustrates one embodiment of a transmission system using a field programmable gate array ("FPGA"). In particular, system 200 comprises a transmission system that ~~interchangers~~ interchanges the time slot allocation of data received or transmitted by the interfaces of system 200 -- i.e. a time division multiplexing system. As illustrated in Figure 2, system 200 comprises a plurality of framers F211 - F21N (block 210) coupled to a FPGA (220) via lines 215a and 215b. FPGA 220, in turn, is coupled to a plurality of digital signal processors (DSP bank 230 - 250) via time slot inter-changers (TSIs 225 - 227). For one embodiment, both DSP bank 230 and DSP bank 240 comprise six DSPs. For another embodiment, DSP bank 250 comprises 24 DSPs. For yet another embodiment, each TSI comprises a non-blocking switch that switches data between sixteen inputs and sixteen outputs, alternatively sixteen input/outputs ("I/Os"). Additionally, each TSI may operate in a minimum delay mode or a constant delay mode. In the minimum delay mode the TSIs transfer data in the same frame the data is received. In the constant delay mode, however, the TSIs transfer data in a subsequent frame from which the data is received.

Please replace the paragraph that begins on page 13, line 3, with the following paragraph:

As previously described, controller 290 uses the host table to determine the number of available unused time slots. In particular, controller 290 uses the host table and the operational characteristics of DSP bank 230 - 250 and TSIs 225 - 227 to determine the number of available unused time slots in system 200. For example, for one embodiment, DSP bank 230 - 250 includes thirty-six DSPs. Each of the DSPs may transmit data on one of sixty-four time slots. In the present example, however, controller 290 only uses the first sixteen time slots of a ~~give~~ given DSP to set up a call connection. Additionally, in the present example, for each frame a TSI may transfer 128 time slots of data between a given input and a given output. Thus, if the time slots of all the framers (F211 - F21n) and DSPs are used to set up call connections, system 200 comprises the following unused time slots:

Please replace the paragraph that begins on page 13, line 17, with the following paragraph:

For another example, each of the framers (F211 - F21N) transfer both voice and control signals. Thus, the framers may transfer 384 time slots -- (2) (8 framers)(24 time slots). Accordingly, if the timeslots of all the framers (F211 - F21n) and DSPs time slots are used to set up call connections, system 200 comprises 1088 unused time slots.

Please replace the paragraph that begins on page 17, line 6, with the following paragraph:

As previously described, FPGA 400 allows system 200 to either transparently transfer a TDM stream or ~~transmits~~ transmit test data in an unused time slot of the TDM stream. After the test data is routed across a connection path, the test data is latched by receiver 440. For one embodiment, controller 290 transmits a latch signal to receiver 440 via control 420. In response to the latch signal, receiver 440 latches data from an unused time slot transmitted on line 470. Subsequently, receiver 440 compares the latched data to the transmitted test data. For one embodiment, receiver 440 uses a logic comparator to compare the latched data to the transmitted test data. For another embodiment, receiver 440 uses exclusive-or gates to compare the latched data to the transmitted test data.

Please replace the paragraph that begins on page 20, line 3, with the following paragraph:

For one embodiment, controller 290 identifies the unused time slots using a host table. In particular, the host table includes a list of time slots that is updated as call connections are set up and removed between the interfaces of system 200. Thus, controller 290 uses the host table list of time slots to identify the unused time ~~slot~~ slots of system 200. After the unused time slots are identified block 520 is processed.